Attorney Docket: M-9564 US

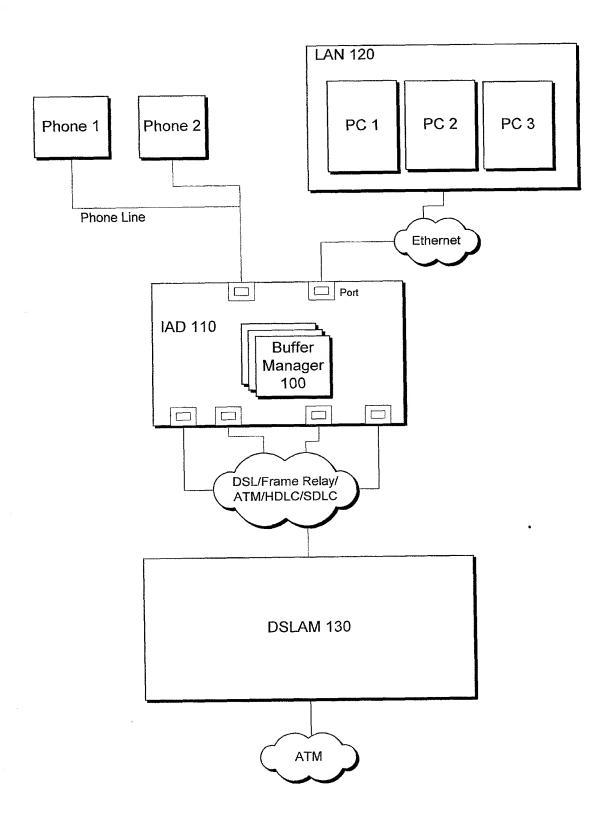


FIG. 1

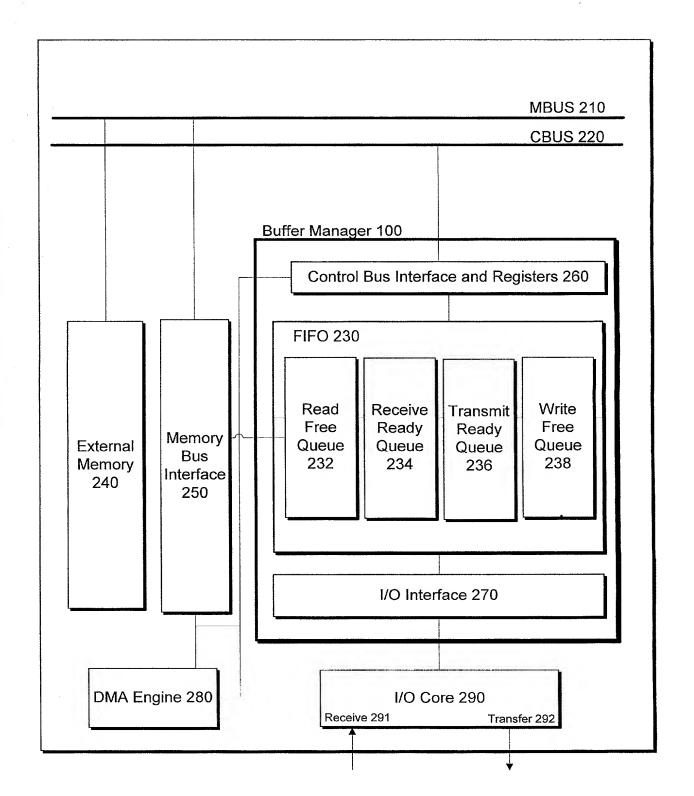
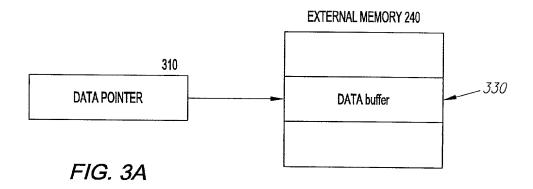


FIG. 2



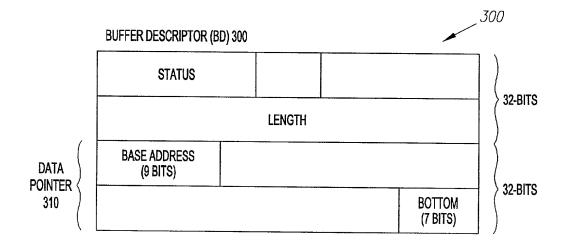
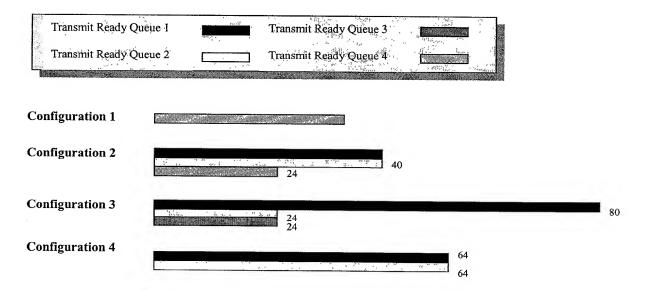


FIG. 3B

Buffer Management For Communication Systems Inventors: Omkar S. Sangha, Ed Kwon, Vijay Maheshwari, Akihiro Kiuchi Serial No.: 09/770,937 Filed: January 25, 2001 Attorney Docket: M-9564 US

Configuration	Bit 8	Bit 7	Transmit Queue#	Depth
1	0	0	1-4	32
2	0	1	1-2	40
			3-4	24
3	1	0	1	80
			2-3	24
			4	0
4	1	1	1	64
			2	64
			3	0
			4	0

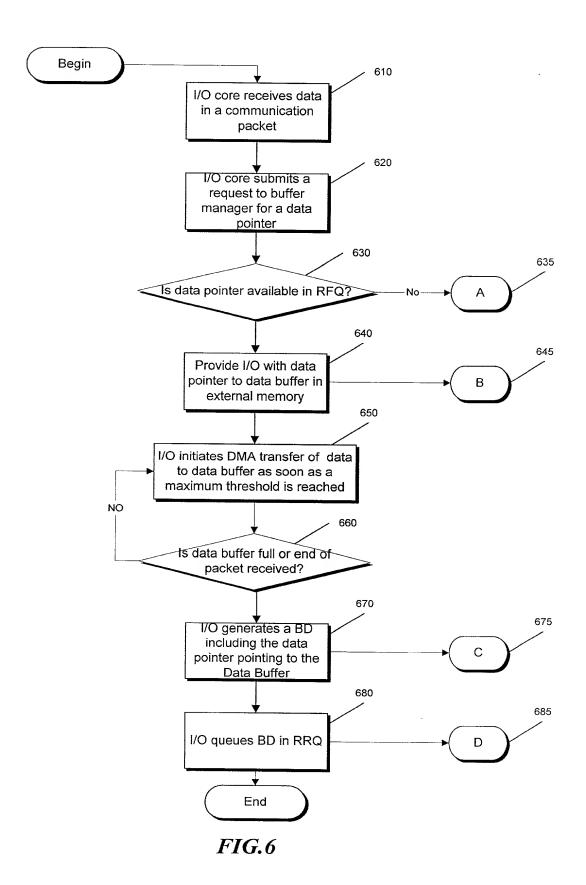
Transmit Ready Queue Configuration



Buffer Management For Communication Systems
Inventors: Omkar S. Sangha, Ed Kwon, Vijay Maheshwari, Akihiro Kiuchi
Serial No.: 09/770,937
Filed: January 25, 2001
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CPU 1/0 CPU 1/0 PORT A PORT A READ FREE QUEUE FIFO RRQ TRQ 64 x 46 64 x 46 64 x 32 128 x 32 256 x 46 BIT BIT BIT BIT BIT **DUAL PORT DUAL PORT** WRITE **MEMORY MEMORY** FREE QUEUE FIFO 510 520 (x4)**RRQ** TRQ 64 x 32 64 x 46 64 x 46 BIT BIT BIT PORT B PORT B DRAM DRAM (EXPANSION MODE)

FIG. 5



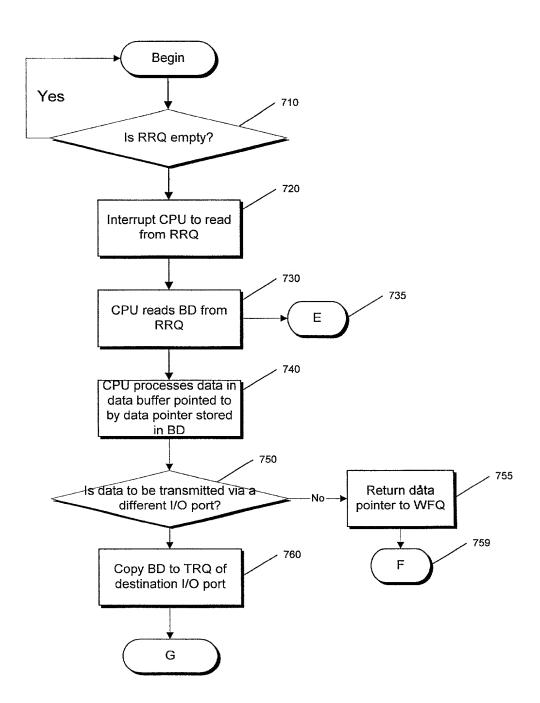


FIG. 7

Serial No.: 09/770,937 Filed: January 25, 2001 Attorney Docket: M-9564 US

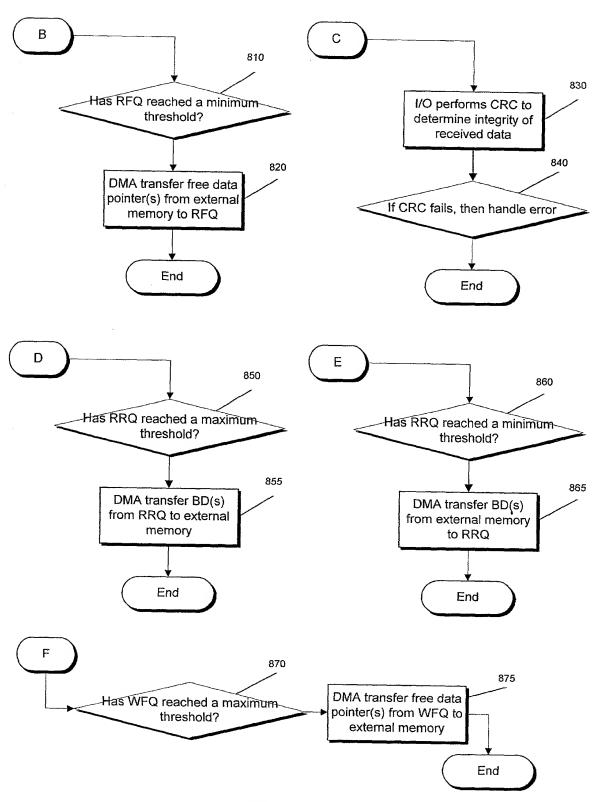
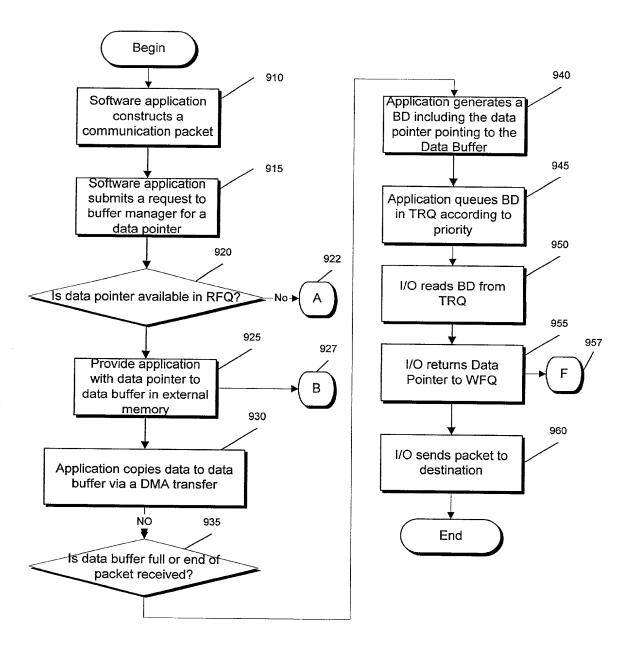
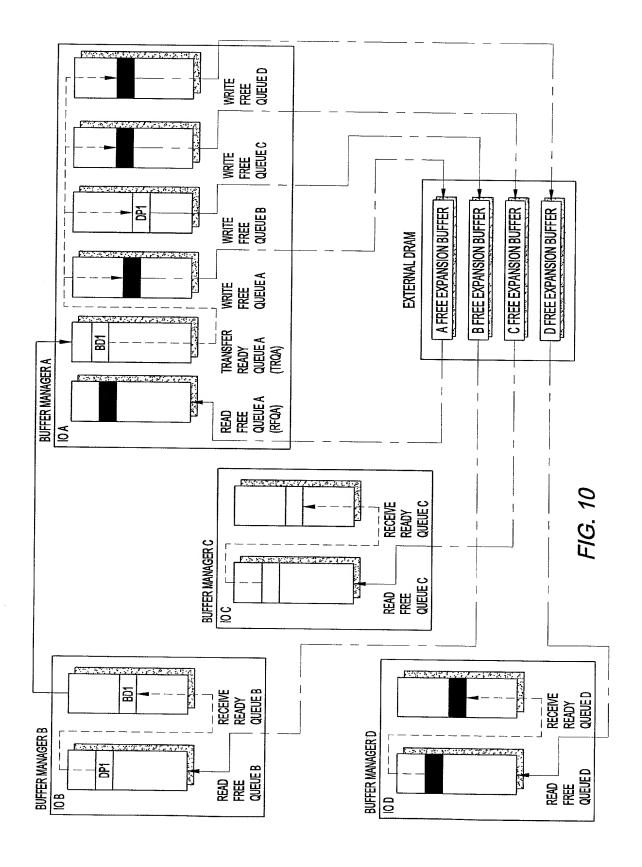


FIG.8

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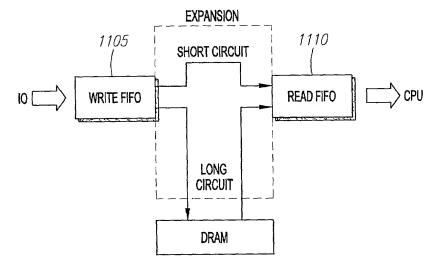


FIG. 11

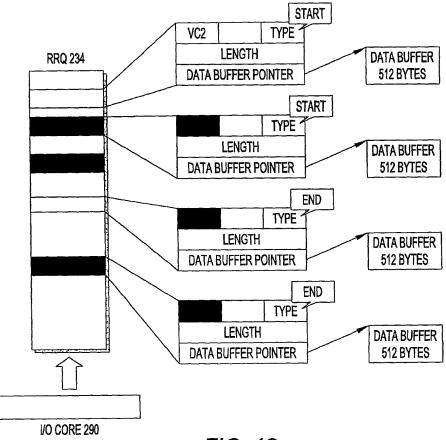


FIG. 12

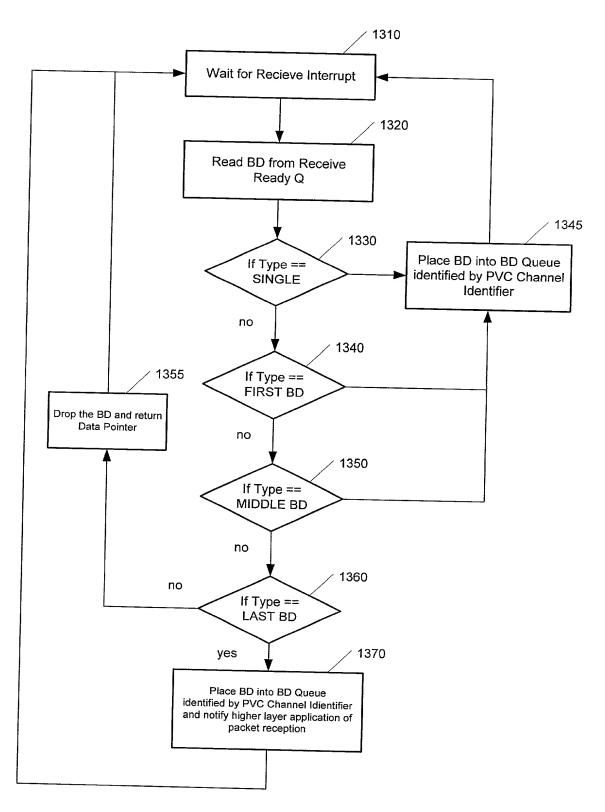


FIG. 13

Serial No.: 09/770,937 Filed: January 25, 2001 Attorney Docket: M-9564 US

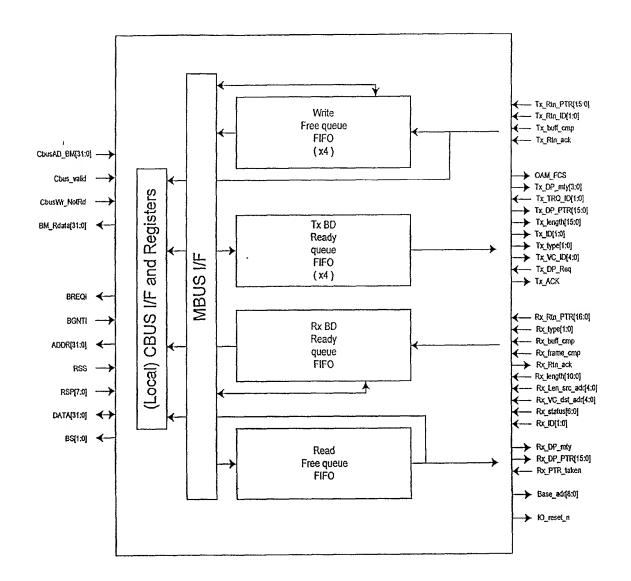


FIG. 14